CMOS, 125 MHz Complete DDS Synthesizer

AD9850

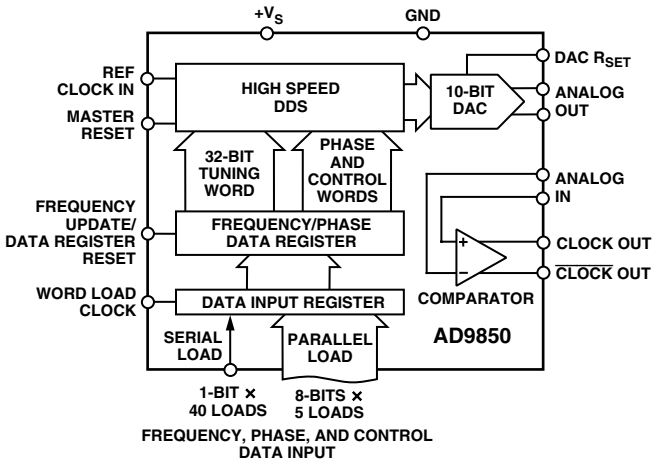
FEATURES

125 MHz Clock Rate
On-Chip High Performance DAC and High Speed Comparator
DAC SFDR > 50 dB @ 40 MHz A_{OUT}
32-Bit Frequency Tuning Word
Simplified Control Interface: Parallel Byte or Serial Loading Format
Phase Modulation Capability
+3.3 V or +5 V Single Supply Operation
Low Power: 380 mW @ 125 MHz (+5 V)
155 mW @ 110 MHz (+3.3 V)
Power-Down Function
Ultrasmall 28-Lead SSOP Packaging

APPLICATIONS

Frequency/Phase–Agile Sine-Wave Synthesis
Clock Recovery and Locking Circuitry for Digital Communications
Digitally Controlled ADC Encode Generator
Agile Local Oscillator Applications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9850 is a highly integrated device that uses advanced DDS technology coupled with an internal high speed, high performance, D/A converter and comparator, to form a complete digitally programmable frequency synthesizer and clock generator function. When referenced to an accurate clock source, the AD9850 generates a spectrally pure, frequency/phase-programmable, analog output sine wave. This sine wave can be used directly as a frequency source or converted to a square wave for agile-clock generator applications. The AD9850's innovative high speed DDS core provides a 32-bit frequency tuning word, which results in an output tuning resolution of 0.0291 Hz, for a 125 MHz reference clock input. The AD9850's circuit architecture allows the generation of output frequencies of up to one-half the reference clock frequency (or 62.5 MHz), and the output frequency can be digitally changed (asynchronously) at a rate of up to 23 million new frequencies per second. The device also provides five bits of digitally controlled phase modulation, which enables phase shifting of its output in increments of 180°, 90°, 45°, 22.5°, 11.25° and any combination thereof. The AD9850 also contains a high speed comparator that can be configured to accept the (externally) filtered output of the DAC to generate a low jitter square wave output. This facilitates the device's use as an agile clock generator function.

The frequency tuning, control, and phase modulation words are loaded into the AD9850 via a parallel byte or serial loading format. The parallel load format consists of five iterative loads of an 8-bit control word (byte). The first byte controls phase modulation, power-down enable, and loading format; bytes 2–5 comprise the 32-bit frequency tuning word. Serial loading is accomplished via a 40-bit serial data stream on a single pin. The AD9850 Complete-DDS uses advanced CMOS technology to provide this breakthrough level of functionality and performance on just 155 mW of power dissipation (+3.3 V supply).

The AD9850 is available in a space saving 28-lead SSOP, surface mount package. It is specified to operate over the extended industrial temperature range of –40°C to +85°C.

REV. E

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